

Sequential System

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Digital Logic for Computer

CS 2302-80

SP-2

Index

Cover Page……………………………………………………………………………………….1

Original Problem…………………………………………………………………………………2

Introduction………………………………………………………………………………………4

System Architecture…………………………………………………………………………….. 5

Subsytem Circuit…………………………………………………………………………………6

Design Validation and Circuit Verification………………………………………………………7

Timing Problems…………………………………………………………………………………8

Alternative Designs………………………………………………………………………………9

Conclusion………………………………………………………………………………………10

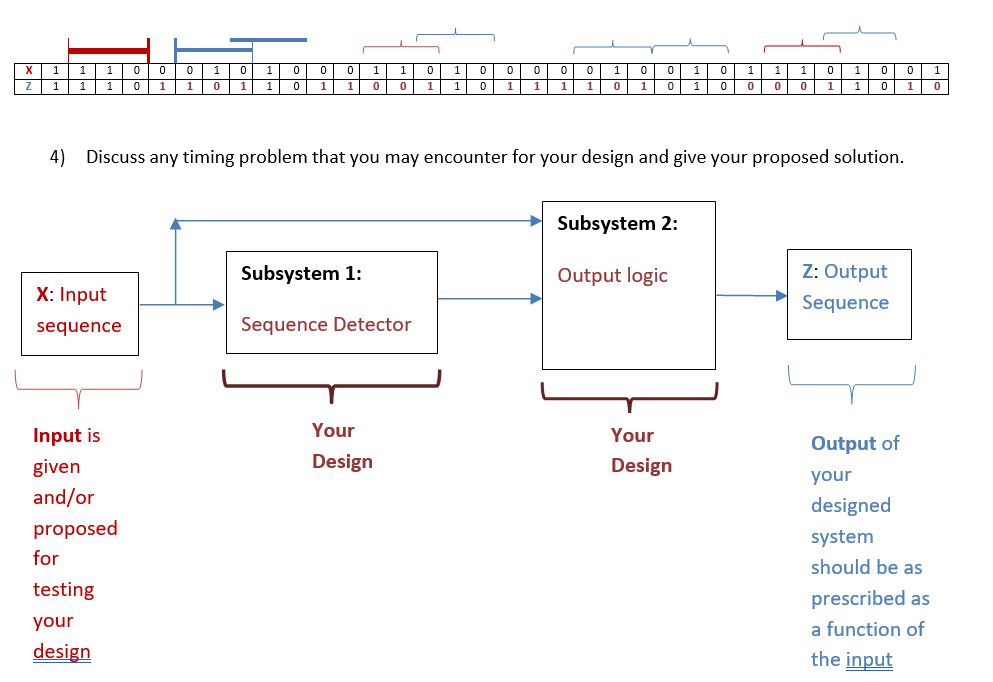
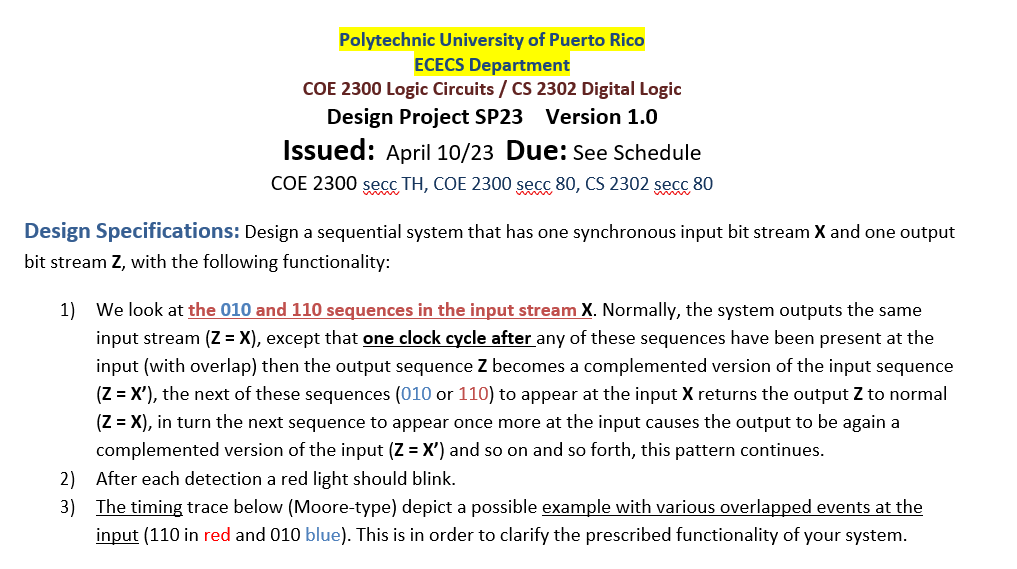
Bibliography……………………………………………………………………………………..11

Functional Groups……………………………………………………………………………….12

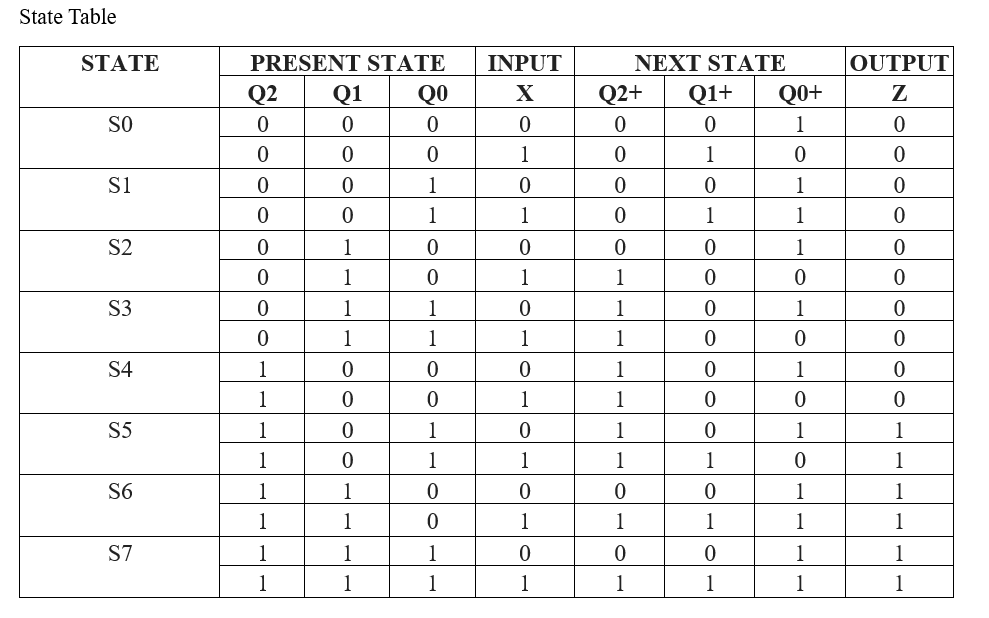
Team Organizational Structure…………………………………………………………………..13

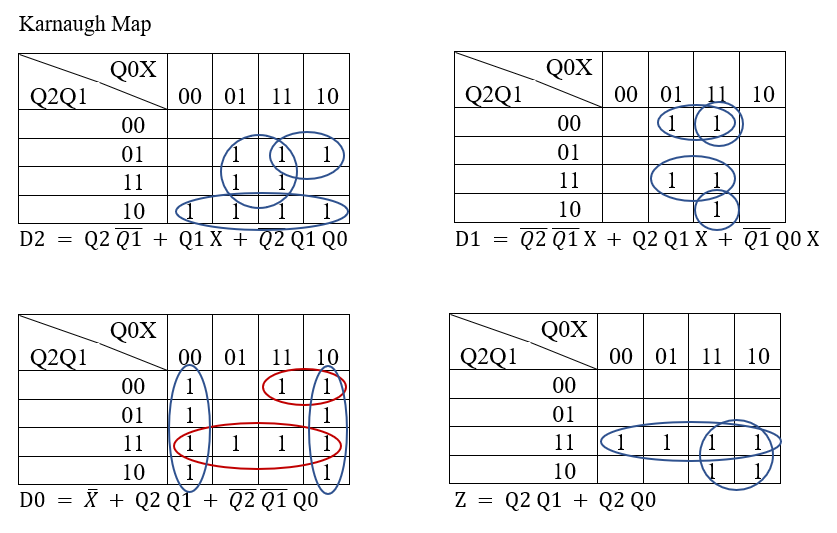
Provide Team Design Rules……………………………………………………………………...14

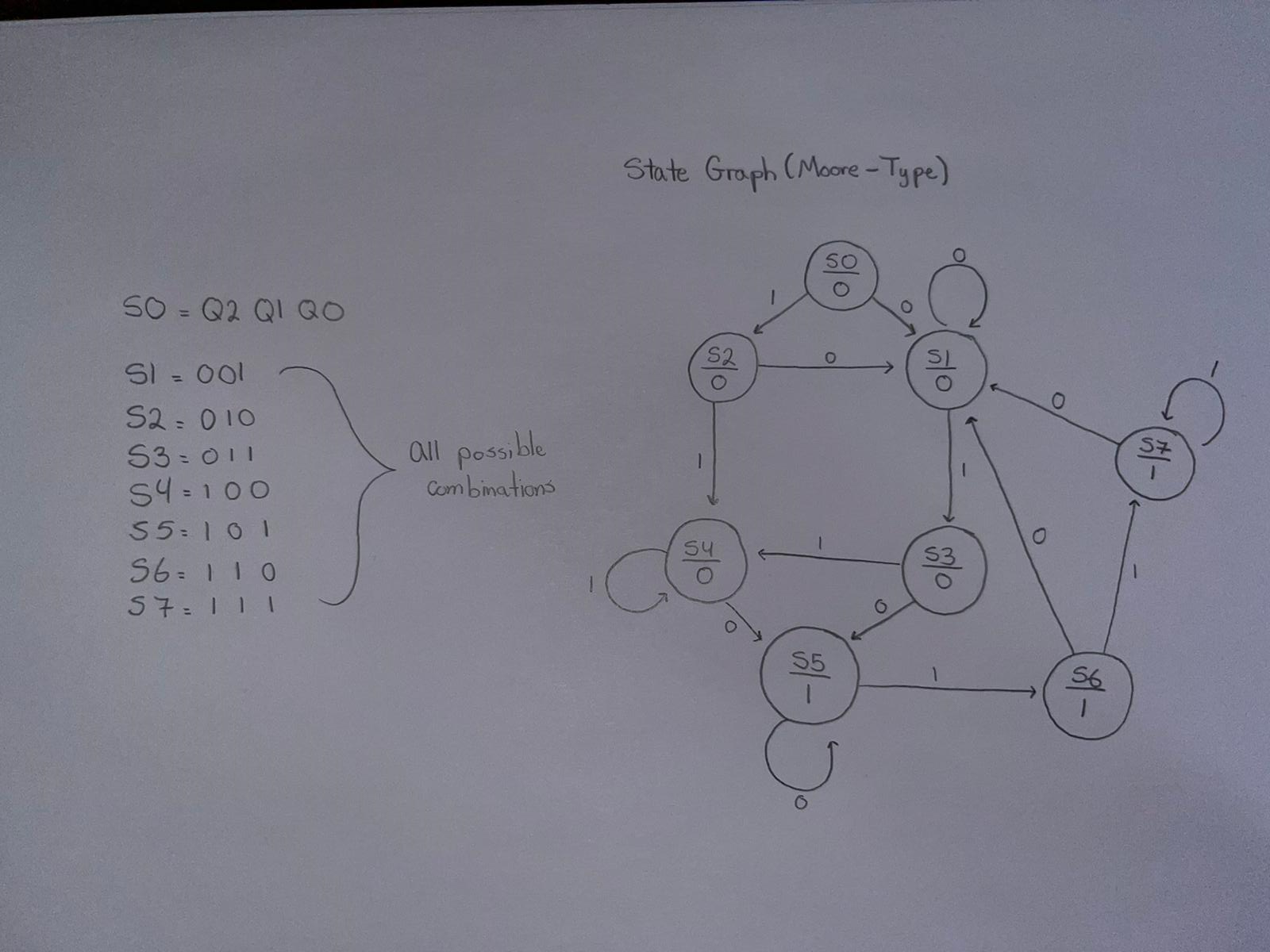
Project Management……………………………………………………………………………..15



System Architecture







Bibliography

Functional Groups

Overall Design Architecture (Logisim)- Derek, Valeria

Circuit Synthesis (VHDL)- Jose Roca, Jose Velez

Simulation- Valeria

Testing- Coral, Jose Roca

Team Organization Structure

Project Leader- Derek

Senior Designer 1- Valeria

Senior Designer 2- Jose Velez

Senior Designer 3 - Coral

Validation Engineer- Jose Roca

**Milestone Compliance (instructor use)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Milestone / Level** | **Not Completed** | **Partially Completed** | **Completed with Corrections** | **Fully Completed** |
| **I** |  |  |  |  |
| **II** |  |  |  |  |
| **III** |  |  |  |  |